Detailed Syllabus
Lecture-wise Breakup

Course Code	19M12EC111	**Semester** : Even 2020 **(specify Odd/Even)**	**Semester** IInd **Session** 2019 -2020 **Month from Jan – May 2020**
Course Name	Adaptive Filters		
Credits	3	**Contact Hours**	3

Faculty (Names)	**Coordinator(s)**	Dr. Vikram Karwal
	Teacher(s) (Alphabetically)	Dr. Vikram Karwal

COURSE OUTCOMES		**COGNITIVE LEVELS**
C152.1	The course aims to familiarize student with need of adaptive systems and their properties	Understanding Level (C2)
C152.2	The course helps students to study algorithms useful for optimization of adaptive systems such as Stochastic Gradient Algorithms	Analyzing Level (C4)
C152.3	The course helps students evaluate the performance of adaptive system such as convergence rates and mean-square error criterion	Evaluating Level (C5)
C152.4	The course helps student design adaptive systems for real time stochastic systems	Applying Level (C3)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	Review and Background Material	Linear Algebra: Hermitian and Positive-Definite Matrices, Schur Complements, Cholesky Factorization, QR Decomposition, Kronecker Products, Complex-Valued Random Variables, Vector-valued Random vectors, Complex Gradients, Cauchy-Riemann Conditions	5
2.	Linear Estimation	Estimation without observations, Estimation given dependent observations, Orthogonality Principle, Spherically Invariant Gaussian Variables, Mean-Square Error Criterion, Minimization by Completion-of-Squares, Minimization of error covariance matrix, Optimal Liner Estimators, Channel Estimation, Block Data Estimation, Linear Channel Equalization, Multiple-Antenna Receivers	7
3.	Constrained Estimation	Minimum-Variance Unbiased Estimation, Mean Estimation, Channel and Noise Estimation, Decision Feedback Equalization, Antenna Beamforming, Recursion for the state Estimator, Riccati Recursion, Measurement and Time-Update Form	8
4.	Stochastic Gradient Algorithms	Principle and Application, Steepest Descent Algorithm, Applications of Adaptive filters, Modes of convergence, Optimal Step size, Weight error vector convergence, Learning curve, contour curves of the Error surface, Iteration-Dependent Step-size, Newton’s method	8

5.	LMS Algorithm	Instantaneous Approximation, Computational cost, Least-perturbation property, Applications: Adaptive Channel Estimation and adaptive Channel Equalization, Decision-Feedback Equalization, Ensemble –Average Learning Curves	6
6.	Least-Squares methods	Least-Squares Problem, Properties and Projection Matrices, Weighted Least-Squares, Regularized Least-Squares, Weighted Regularized Least-Squares, RLS Algorithm, Regularization,	6
		Total number of Lectures	**40**

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25 (5 Assignment, 5 Quiz, 5 Class Participation, 10 Attendance)
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Adaptive Filters by Ali H Sayed
2.	Symon Haikin Adaptive Filters

Detailed Syllabus
Lecture-wise Breakup

Subject Code	18M12EC111	**Semester:** EVEN	**Semester :** II **Session** 2020 **Month from :** January to May
Subject Name	ASIC Verification using System Verilog		
Credits	**3**	**Contact Hours**	**3-0-0**

Faculty (Names)	**Coordinator(s)**	1. Dr. Shruti Kalra
	Teacher(s)	2.

COURSE OUTCOMES		**COGNITIVE LEVELS**
C151.1	Recall the basics and need of ASIC verification	Remembering Level (C1)
C151.2	Understand the concepts of verilog and system verilog	Understanding Level (C2)
C151.3	Applying system verilog to code, simulate and verify the system	Applying Level (C3)
C151.4	Analyze the verification environment to build and verify DUT through testbenches.	Analyzing Level (C4)

Module No.	Title of the Module	Topics in the Module	No. of Lectures for the module
1.	**Introduction**	ASIC Design Flow, Validation vs. Verification, Verification Model, Hardware Verification Languages, Phases of Verification, Verification Infrastructure – Stimulus Generator, Driver, Scoreboard, DUT and Monitor, Functional coverage, Code Coverage – Statement, Path, Expression, FSM Coverage, Assertions, Chip Testing – Boundary Scan, BIST	3
2.	**Verilog**	Introduction, Verilog Module, Module Instantiation, Data Types – Reg, Wire; Verilog Operators – Arithmetic, Logical, Relational, Equality, Reduction, Bitwise; Modelling – Structural, Behavioural and Dataflow, Control Statements, Initial Block, Always Block; Function, Task, Blocking Vs.Non-Blocking, Logic synthesis, Simulation Synthesis Mismatch	11
3.	**System Verilog**	Introduction, Features, Module, Data Types – 2 valued & 4 valued; Arrays, Logic Operators & their types; Fork Join Statement and their types; Random Number Generation; SV Packages; Tasks & functions; SV Parameters; SV Test Bench; Race Condition; Clocking Block	10
4.	**Test Bench & Verification Environment using System verilog**	Test Bench Model, Directed Tests, Random Verification, Linear Test Bench, Linear Random Test Bench, Self-Checking Test Bench; Module Instantiation Methods; Stimulus Techniques – Using Initial Block, Always Block, Array of Vectors, & Forced Stimulus; Verification Environment Hierarchy – Stimulus Class, Driver Class,	14

		Monitor Class, Scoreboard, Checkers etc	
5	**System verilog Assertions & Coverage**	Covergroups, coverpoints, coverage groups, coverpoinmt expressions, coverage bins, explicit bin creation, transition bins, wildcard bins, ignore bins, illegal bins, cross coverage, coverage methods, cover property, SV assertions and types	4
		Total number of Lectures	42

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	System Verilog for verification by Chris Spear, 3rd Edition, Springer, 2008
2.	Mintz, Mike, and Robert Ekendahl. Hardware Verification with System Verilog: An Object-Oriented Framework. Vol. 230. Springer Science & Business Media, 2007.
3.	Simkov, Marcela. Hardware Accelerated Functional Verification: Framework for FPGA-Accelerated Functional Verification. LAP Lambert Academic Publishing, 2011.

Detailed Syllabus
Lecture-wise Breakup

Subject Code	17M21EC115	**Semester** Even	**Semester** II **Session** 2019-20 **Month from** January to May
Subject Name	Analogue Integrated Circuit Design		
Credits	3	**Contact Hours**	3

Faculty (Names)	**Coordinator(s)**	Dr. Saurabh Chaturvedi
	Teacher(s) (Alphabetically)	Dr. Saurabh Chaturvedi

COURSE OUTCOMES - At the end of the course, students will be able to		**COGNITIVE LEVELS**
C115.1	Relate and recall the MOS device physics	Remembering Level (C1)
C115.2	Understand the concepts of single-stage amplifiers, differential amplifiers and current mirrors	Understanding Level (C2)
C115.3	-Apply the phenomenon of noise and its effects on analogue circuits -Apply various feedback topologies in analogue circuits	Applying Level (C3)
C115.4	Analyze the multistage CMOS amplifiers (op amps) and voltage references	Analyzing Level (C4)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures**
1.	Basic MOS device physics	MOSFET structures and symbols, MOSFET I-V characteristics, Second-order effects, Device models	6
2.	Single-stage amplifiers	Basic concepts, Small-signal model, Common-source stage, Source follower, Common-gate stage, Cascode stage, Frequency response of amplifiers	6
3.	Differential amplifiers	Single-ended and differential operations, Basic differential pair, Common-mode response	5
4.	Current mirrors	Basic current mirrors, Cascode current mirrors, Active current mirrors	5
5.	Noise in analogue circuits	Noise characteristics and spectrum, Types of noise, Representation of noise in circuits, Noise bandwidth	6
6.	Feedback	Properties of feedback circuits, Feedback topologies, Effect of loading	5
7.	Operational amplifiers	Performance parameters, One-stage op amps, Two-stage op amps, Gain boosting, Slew rate	5
8.	Bandgap references	General considerations, Supply-independent biasing, Temperature-independent references, PTAT current generation, Constant-G_m biasing	4

	Total Number of Lectures	**42**
Evaluation Criteria **Components** **Maximum Marks** T1 20 T2 20 End Semester Examination 35 TA 25 **Total** **100**		

Recommended Reading Material:	
1.	B. Razavi, *Design of analog CMOS integrated circuits*, 2nd ed., McGraw-Hill Education, 2017.
2.	P. E. Allen and D. R. Holberg, *CMOS analog circuit design*, 3rd ed., Oxford University Press, 2015.
3.	P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and design of analog integrated circuits*, 5th ed., John Wiley & Sons, 2014.

Detailed Syllabus

Lecture-wise Breakup

Subject Code	**17M21EC113**	**Semester Even**	**Semester 2nd & 9th Session** 2019-20 **Month from** Jan 20 to Jun 20
Subject Name	**Project Based Learning - I**		
Credits	2	**Contact Hours**	2

Faculty (Names)	**Coordinator(s)**	Dr. Gaurav Verma
	Teacher(s) (Alphabetically)	NA

COURSE OUTCOMES		**COGNITIVE LEVELS**
C190.1	Summarize the contemporary scholarly literature, activities, and explored tools/ techniques/software/hardware for hands-on in the respective project area in various domain of Embedded Systems, Signal Processing, VLSI, Communication, Artificial Intelligence and Machine Learning/Deep Learning etc.	Understanding (Level II)
C190.2	Analyze/ Design the skill for obtaining the optimum solution to the formulated problem with in stipulated time	Analysing (Level IV)
C190.3	Use latest techniques and software tools for achieving the defined objectives.	Evaluating (Level V)
C190.4	Evaluate /Validate sound conclusions based on evidence and analysis.	Evaluating (Level V)

Evaluation Criteria

Components	**Maximum Marks**
Mid Sem Evaluation	40
Final Evaluation	40
Report	20
Total	**100**

Detailed Syllabus
Lecture-wise Breakup

Course Code	17M21EC114	**Semester** EVEN **(specify Odd/Even)**	**Semester** II (M.Tech.) & VIII (INTG.) **Session** 2019 -2020 **Month from:** January to June
Course Name	Advanced Embedded Systems		
Credits	4	**Contact Hours**	3L

Faculty (Names)	**Coordinator(s)**	Dr. Gaurav Verma (62)
	Teacher(s) (Alphabetically)	

COURSE OUTCOMES		**COGNITIVE LEVELS**
C114.1	**Understanding of the fundamental concepts of ARM7 processor and detailed study of complete architecture of the ARM7 based LPC2148 microcontroller.**	Level (C3)
C114.2	**Understanding and detailed study of the complete architecture of the ARM-CORTEX processor and STM32 (ARM-CORTEX based microcontroller).**	Level (C2)
C114.3	**Experiment the basic concepts of embedded 'C' programming to program on chip and external peripherals with STM32 microcontroller around various sensors and actuators.**	Level (C4)
C114.4	**Understanding of the basic concept of Linux Operating system and Linux system programming using 'C'**	Level (C2)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	ARM7TDMI Architecture & On Chip Peripherals (LPC2148)	Review of ARM architecture, System Peripherals, Memory Accelerated Module (MAM), Phase Locked Loop (PLL), Power Control, APB (ARM Peripheral Bus) Divider, Wake up Timer, Brown out detection, Pin Connect Block, Interrupt System, Vectored Interrupt Controller (VIC), User Peripherals, General Purpose Input/ Output (GPIO), Timer/Counter, Pulse Width Modulation (PWM), Real Time Clock (RTC), Watch Dog Timer (WDT), ADC & DAC, On Chip Communication Interface, Universal Asynchronous Receiver Transmitter (UART), Inter Integrated Communication (I2C), Serial Peripheral Interface (SPI).	12
2.	ARM CORTEX Processor (M3) and Controller (STM32)	ARM Architectural Revision, Cortex Processor And Cortex CPU, Cortex CPU Pipeline, Programmer's Model CPU Operating Modes, Thumb-2 Instruction Set, Memory Map, Unaligned Memory Accesses, Bit Banding Cortex Processor Busses, Bus Matrix, System Timer, Interrupt Handling, Nested Vector Interrupt Controller, STM32 Family, Package Types & Portfolio, Features of STM32F100RB, STM32 Architecture& pin description, Hardware Considerations,	12

		Memory map & bus structure, External Oscillators, Clock control and Internal Oscillators.	
3.	On chip peripherals of STM32F100RB	Reset and Clock Control Group, Phase Locked Loop (PLL), APB1 and APB2 (ARM peripheral Bus) divider, GPIOs & AFIOs (General purpose input output), Timer/Counter (Basic and General Purpose), Capture and Compare mode of Timers, PWM (Pulse Width modulation), DMA (Direct Memory Access, Interfacing with sensors and actuators	10
4.	Linux Basics & System Programming	Linux Basics, Introduction to Linux, Reasons for its popularity, Linux file system, Linux Distributions, Linux Commands, Operating System architecture and concepts, Kernel classification (Monolith kernel and Microkernel), Linux System Programming, Working with files (high & low level file handling).	8
		Total number of Lectures	**42**

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25 (Assignments and Quiz)
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	http://www.**hitex**.com/fileadmin/pdf/insiders.../**stm32/**isg-**stm32**-v18d-scr.pdf.
2.	http://www.hitex.com/fileadmin/pdf/insiders-guides/lpc/lpc-arm-book_rev10-screen.pdf
3.	Neil Matthew / Richard Stones, "Beginning Linux Programming", Wrox India, 2002.
4.	Robert Love, "Device Drivers", 1st Edition, O'Reilly, 2010.

Detailed Syllabus
Lab-wise Breakup

Course Code	17M25EC112	**Semester:** Even **(specify Odd/Even)**	**Semester:** 2nd **Session** 2019-20 **Month from:** January to June
Course Name	VLSI Design & Simulation Lab		
Credits	2	**Contact Hours**	6

Faculty (Names)	**Coordinator(s)**	Dr. Akansha Bansal
	Teacher(s) (Alphabetically)	Dr. Akansha Bansal, Dr. Shruti Kalra

COURSE OUTCOMES - At the end of the course, students will be able to:		**COGNITIVE LEVELS**
C173.1	Familiarize with the VLSI CAD tools	Understanding Level (C2)
C173.2	Structure creation & Visualization of VLSI devices and systems	Applying Level (C3)
C173.3	Characterize and validation of VLSI devices and systems	Applying Level (C3)

Module No.	List of Experiments	CO
1.	Introduction to Structure creation tools (SDE & SPROCESS) Sentaurus TCAD	C173.1
2.	Introduction to structure characterization (SDEVICE) and Structure visualization (SVISUAL) Tool	C173.1
3.	PN junction diode structure creation using GUI SDE	C173.2
4.	PN junction diode structure characterization using SDEVICE	C173.3
5.	MOS capacitor creation using GUI SDE	C173.2
6.	MOS capacitor characterization using SDEVICE	C173.3
7.	MOSFET creation using GUI SDE	C173.2
8.	MOSFET characterization using SDEVICE	C173.3
9.	PN junction diode structure creation using SPROCESS & characterization using SDEVICE	C173.2
10.	Variation of various parameters of MOSFET and plot the IV characteristics	C173.3
11.	Write a Verilog description code for 2*4 Decoder	C173.1
12.	Write the Verilog description code of 4*1 MUX using case statement.	C173.1
13.	Write the Verilog description code for JK Flip-Flop**.**	C173.1
14.	Write the Verilog description code of 4- bit full adder.	C173.1
15.	Write the Verilog description code of basic calculator.	C173.1
16.	FSM for sequence detector for sequence 0011	C173.2
17.	HDL description for Full subtractor using structural design	C173.2
18.	HDL description for 4-bit binary to gray code converter	C173.2
19.	HDL description for 1 bit comparator using Data flow design	C173.2

20.	HDL description for 4 bit Parity checker using behavioural design	C173.2
21.	Structure model for full adder using two half adders	C173.2
22.	HDL code for BCD to excess-3 code converter	C173.2
23.	HDL code for 4-bit binary multiplier.	C173.3
24.	HDL code for 4-bit magnitude comparator	C173.3
25,	HDL code for universal shift register	C173.3

Recommended Reading material:	
1.	Sentaurus SDE, SDEVICE, SPROCESS, SVISUAL user manuals
2.	Sentaurus TCAD tutorials
3.	http://www.micro.deis.unibo.it/~rudan/MATERIALE_DIDATTICO/diapositive/TCAD/01_TCAD_laboratory_Introduction_GBB_20150225.pdf