Detailed Syllabus
Lecture-wise Breakup

Subject Code	**17M12EC130**	**Semester (specify Odd/Even)**	**Semester EVEN Session 2018 - 2019 Month from Jan. to June 2019**
Subject Name	Advanced Wireless Networks		
Credits	**3**	**Contact Hours**	**3**

Faculty (Names)	**Coordinator(s)**	1. Pankaj Kumar Yadav
	Teacher(s) (Alphabetically)	1. Pankaj Kumar Yadav

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO1	To review of 2G/GSM Network: Evolution of mobile communication systems, Cellular Concept, GSM Network Architecture. Develop an understanding of the TCP/IP and Mobile telecommunication network models	Remember (Level I)
CO2	To understand the concept of Quality of services (QoS) in data networks. Evaluation wireless data networks (2G/GSM, 3G/UMTS and 3.5G HSPA) architecture in terms of QoS design parameters.	Understand (Level II)
CO3	To analyze the LTE Air Interface and LTE Core Network	Apply (Level III)
CO4	To evaluate happening between different LTE network elements with the help of various Signaling Scenarios.	(Analyze Level IV)

Module No.	**Subtitle of the Module**	**Topics in the module**	**No. of Lectures for the module**
1.	A review of 2G/3G Networks	Evolution of mobile communication systems. GSM: Network Architecture; Call Scenarios. Quality of services (QoS) in data networks. GPRS/EDGE networks evolutions. UMTS: Network Architecture Concept of CDMA; WCDMA Specifications; Peak data calculations for UMTS, HSDPA and HSPA+	12
2.	Overview of LTE	Evolution of LTE; High Level Architecture (LTE Nodes & Interfaces);	8
3.	LTE Air Interface	Principle for OFDM (including Concept of Orthogonality & Concept of CP (Cyclic Prefix)); Principle of SC-FDMA signal and Limitations of Single Carrier Modulation; OFDMA symbols, parameters, Subcarrier Types; Concept of flexible spectrum usage; Downlink Physical signal and channels; Uplink Physical signal and channels; Physical Layer Structure (Frame Structure, RB, Resource Grid); Duplexing and Modulation Schemes in LTE; LTE Radio Interface Protocol Stack; LTE Radio Interface LTE States	12
4.	LTE Core Network (EPC Core)	EPC Core nodes (MME, S-GW, PDN-GW, PCRF etc.); S1 interface; S1AP Protocol; NAS Procedures;	5

5.	LTE Signaling Scenarios	LTE Initial access; Random access procedure; Initial Context setup procedure; Attach/Detach procedure; Service request; Handover and Call Initiatives/ establishment	8
6	LTE-Advanced LTE -A and 5G - Basics	LTE – Advanced: COMP, CA, Relay, Heterogeneous N/w, MU-MIMO, N/w MIMO, LTE-IOT, Introduction to 5G	4
		Total number of Lectures	**40**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	T. S. Rappaport, Wireless Communications, PHI, 2002.
2.	Gunnar Heine, GSM Networks: Protocols, Terminology and Implementation, Artech House, 1999.
3.	Andrea Goldsmith, Wireless Communications, Cambridge University Press, 2005
4.	Harri Holma, Antti Toskala, LTE for UMTS: Evolution to LTE-Advanced, John Wiley and Sons, 2011
5.	5G Technology Evolution Recommendations, 4G Americas, 2015
6	http://www.3gpp.org/ftp/Specs/html-info/36-series.htm

Detailed Syllabus
Lecture-wise Breakup

Course Code	19M12EC111	**Semester** : Even 2019 **(specify Odd/Even)**	**Semester** IInd **Session** 2018 -2019 **Month from Jan – May 2019**
Course Name	Adaptive Filters		
Credits	3	**Contact Hours**	3

Faculty (Names)	**Coordinator(s)**	Dr. Vikram Karwal
	Teacher(s) (Alphabetically)	Dr. Vikram Karwal

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO1	The course aims to familiarize student with need of adaptive systems and their properties	Apply Level (C3)
CO2	The course helps students to study algorithms useful for optimization of adaptive systems such as Stochastic Gradient Algorithms	Analyze Level (C4)
CO3	The course helps students analyze the performance of adaptive system such as convergence rates and mean-square error criterion	Evaluate Level (C5)
CO4	The course helps student design adaptive systems for real time stochastic systems	Create Level (C6)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	Review and Background Material	Linear Algebra: Hermitian and Positive-Definite Matrices, Schur Complements, Cholesky Factorization, QR Decomposition, Kronecker Products, Complex-Valued Random Variables, Vector-valued Random vectors, Complex Gradients, Cauchy-Riemann Conditions	5
2.	Linear Estimation	Estimation without observations, Estimation given dependent observations, Orthogonality Principle, Spherically Invariant Gaussian Variables, Mean-Square Error Criterion, Minimization by Completion-of-Squares, Minimization of error covariance matrix, Optimal Liner Estimators, Channel Estimation, Block Data Estimation, Linear Channel Equalization, Multiple-Antenna Receivers	7
3.	Constrained Estimation	Minimum-Variance Unbiased Estimation, Mean Estimation, Channel and Noise Estimation, Decision Feedback Equalization, Antenna Beamforming, Recursion for the state Estimator, Riccati Recursion, Measurement and Time-Update Form	8
4.	Stochastic Gradient Algorithms	Principle and Application, Steepest Descent Algorithm, Applications of Adaptive filters, Modes of convergence, Optimal Step size, Weight error vector convergence, Learning curve, contour curves of the Error surface, Iteration-Dependent Step-size, Newton's method	8
5.	LMS Algorithm	Instantaneous Approximation, Computational cost, Least-perturbation property, Applications: Adaptive Channel	6

		Estimation and adaptive Channel Equalization, Decision-Feedback Equalization, Ensemble –Average Learning Curves	
6.	Least-Squares methods	Least-Squares Problem, Properties and Projection Matrices, Weighted Least-Squares, Regularized Least-Squares, Weighted Regularized Least-Squares, RLS Algorithm, Regularization,	6
		Total number of Lectures	**40**

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25 (5 Assignment, 5 Quiz, 5 Class Participation, 10 Attendance)
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Adaptive Filters by Ali H Sayed
2.	Symon Haikin Adaptive Filters

Detailed Syllabus
Lecture-wise Breakup

Course Code	18M12EC111	**Semester** Even	**Semester** 2nd (M.Tech) **Session** 2018-19 **Month from** January 2019 to June 2019
Course Name	ASIC Verification using System Verilog		
Credits	3	**Contact Hours**	3 per week

Faculty (Names)	**Coordinator(s)**	Mandeep Singh Narula
	Teacher(s) (Alphabetically)	Mandeep Singh Narula

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO1	Study the need of verification, different phases of verification, and creation of verification infrastructure.	Understanding (Level II)
CO2	Understand code coverage, functional coverage and system verilog assertions	Analysis (Level IV)
CO3	Understand the basic constructs in verilog language and coding style for modeling different circuits	Analysis (Level IV)
CO4	Understand the system verilog enhancements over verilog language and constructs in system verilog	Analysis (Level IV)
CO5	Understand how verification environment is build to verify DUT using different components like driver, generator, scoreboard, monitor etc.	Analysis (Level IV)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	Introduction to ASIC Verification	ASIC Design Flow, Validation vs. Verification, Verification Model, Hardware Verification Languages, Phases of Verification, Verification Infrastructure – Stimulus Generator, Driver, Scoreboard, DUT and Monitor, Functional coverage, Code Coverage – Statement, Path, Expression, FSM Coverage, Assertions, Chip Testing – Boundary Scan, BIST	4
2.	Verilog	Introduction, Verilog Module, Module Instantiation, Data Types – Reg, Wire; Verilog Operators – Arithmetic, Logical, Relational, Equality, Reduction, Bitwise; Modelling – Structural, Behavioural and Dataflow, Control Statements, Initial Block, Always Block; Function, Task, Blocking Vs.Non-Blocking, Logic synthesis, Simulation Synthesis Mismatch	10

3.	System Verilog	Introduction, Features, Module, Data Types – 2 valued & 4 valued; Arrays, Logic Operators & their types; Fork Join Statement and their types; Random Number Generation; SV Packages; Tasks & functions; SV Parameters; SV Test Bench; Race Condition; Clocking Block	10
4.	Test Bench & Verification Environment using System verilog	Test Bench Model, Directed Tests, Random Verification, Linear Test Bench, Linear Random Test Bench, Self-Checking Test Bench; Module Instantiation Methods; Stimulus Techniques – Using Initial Block, Always Block, Array of Vectors, & Forced Stimulus; Verification Environment Hierarchy – Stimulus Class, Driver Class, Monitor Class, Scoreboard, Checkers etc	10
5.	System verilog Assertions & Coverage	Covergroups, coverpoints, coverage groups, coverpoinmt expressions, coverage bins, explicit bin creation, transition bins, wildcard bins, ignore bins, illegal bins, cross coverage, coverage methods, cover property, SV assertions and types	8
		Total number of Lectures	42

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	System Verilog for verification by Chris Spear, 3rd Edition, Springer
2.	Hardware Verification with System Verilog (Authors: Mintz, Mike, Ekendahl, Robert), Springer

Detailed Syllabus
Lecture-wise Breakup

Course Code	17M21EC114	**Semester** EVEN **(specify Odd/Even)**	**Semester** II **Session** 2018 -2019 **Month from:** January to June
Course Name	Advanced Embedded System		
Credits	4	**Contact Hours**	3L

Faculty (Names)	**Coordinator(s)**	Dr. Gaurav Verma (62)
	Teacher(s) (Alphabetically)	

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO1	**Understanding of the fundamental concepts of ARM7 processor and detailed study of complete architecture of the ARM7 based LPC2148 microcontroller.**	Apply Level (C3)
CO2	**Understanding and detailed study of the complete architecture of the ARM-CORTEX processor and STM32 (ARM-CORTEX based microcontroller).**	Understand Level (C2)
CO3	**Experiment the basic concepts of embedded 'C' programming to program on chip and external peripherals with STM32 microcontroller around various sensors and actuators.**	Analyze Level (C4)
CO4	**Understanding of the basic concept of Linux Operating system and Linux system programming using 'C'**	Understand Level (C2)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	ARM7TDMI Architecture & On Chip Peripherals (LPC2148)	Review of ARM architecture, System Peripherals, Memory Accelerated Module (MAM), Phase Locked Loop (PLL), Power Control, APB (ARM Peripheral Bus) Divider, Wake up Timer, Brown out detection, Pin Connect Block, Interrupt System, Vectored Interrupt Controller (VIC), User Peripherals, General Purpose Input/ Output (GPIO), Timer/Counter, Pulse Width Modulation (PWM), Real Time Clock (RTC), Watch Dog Timer (WDT), ADC & DAC, On Chip Communication Interface, Universal Asynchronous Receiver Transmitter (UART), Inter Integrated Communication (I2C), Serial Peripheral Interface (SPI).	12
2.	ARM CORTEX Processor (M3) and Controller (STM32)	ARM Architectural Revision, Cortex Processor And Cortex CPU, Cortex CPU Pipeline, Programmer's Model CPU Operating Modes, Thumb-2 Instruction Set, Memory Map, Unaligned Memory Accesses, Bit Banding Cortex Processor Busses, Bus Matrix, System Timer, Interrupt Handling, Nested Vector Interrupt Controller, STM32 Family, Package Types & Portfolio, Features of STM32F100RB, STM32 Architecture& pin description, Hardware Considerations,	12

		Memory map & bus structure, External Oscillators, Clock control and Internal Oscillators.	
3.	On chip peripherals of STM32F100RB	Reset and Clock Control Group, Phase Locked Loop (PLL), APB1 and APB2 (ARM peripheral Bus) divider, GPIOs & AFIOs (General purpose input output), Timer/Counter (Basic and General Purpose), Capture and Compare mode of Timers, PWM (Pulse Width modulation), DMA (Direct Memory Access, Interfacing with sensors and actuators	10
4.	Linux Basics & System Programming	Linux Basics, Introduction to Linux, Reasons for its popularity, Linux file system, Linux Distributions, Linux Commands, Operating System architecture and concepts, Kernel classification (Monolith kernel and Microkernel), Linux System Programming, Working with files (high & low level file handling).	8
		Total number of Lectures	**42**

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25 (Assignments and Quiz)
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	http://www.**hitex**.com/fileadmin/pdf/insiders.../**stm32**/isg-**stm32**-v18d-scr.pdf.
2.	http://www.hitex.com/fileadmin/pdf/insiders-guides/lpc/lpc-arm-book_rev10-screen.pdf
3.	Neil Matthew / Richard Stones, "Beginning Linux Programming", Wrox India, 2002.
4.	Robert Love, "Device Drivers", 1st Edition, O'Reilly, 2010.

Detailed Syllabus
Lecture-wise Breakup

Course Code	17M21EC115	**Semester :** Even **(specify Odd/Even)**	**Semester** II **Session** 2018 -2019 **Month from Jan to May**
Course Name	Analogue Integrated Circuit Design		
Credits	3	**Contact Hours**	**3**

Faculty (Names)	**Coordinator(s)**	Dr Garima Kapur
	Teacher(s) (Alphabetically)	Nil

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO1	To remember and understand prerequisite topics like MOS physics and circuits.	Understanding (Level II)
CO2	To analyze noise and applying various feedback topologies removing it.	Analyzing (Level IV)
CO3	To classify and design Differential Amplifier	Analyzing (Level IV)
CO4	To Analyze Multistage Amplifier like Opamp. Design Voltage references	Evaluating (Level V)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	Basic MOS Physics, CMOS Technology	MOS IV Characteristics, Second order Effects, MOS Device Models, Introduction and Overview of IC technology, small signal models, Single stage Amplifiers - gain and bias considerations; Current Sources, Current mirrors, Cascade current mirrors; Frequency response of Amplifier – CS Amplifer, Miller effect	12
2.	Noise in Analog Circuits	Noise Characteristics, Thermal Noise, Flicker Noise, Representation of Noise in Circuits, Noise in Single Stage CS, CD, CG Amplifiers, Noise in Differential Pairs, Noise Bandwidth	08
3.	Feedback	Properties of Feedback Circuits, Feedback Topologies – Voltage-voltage, Current-voltage, Voltage-current, Current-current, Effect of Loading on Feedback Topologies,	06
4.	Differential Amplifiers	Single-ended and Differential Operation, basic Differential Amplifier pair – DC, AC and Transient Analysis, Common-Mode Response	04
5.	Operational Amplifier Design	Closed –loop stability of op-amp , Two stage opamp with miller compensation, differential and common mode half circuits, common mode feedback; Fully	06

		differential miller compensated opamp; Folded cascode Op-Amp design	
6.	Bandgap References	PTAT, CTAT, Bandgap References, Low power design techniques	04
		Total number of Lectures	**40**

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25 (15:Att+ 10:Assign.)
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Behazd Razavi, "The Design of Analog CMOS Integrtaed Circuits", 2nd edition, McGrawHill, 2001
2.	Philip Allen, D. Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford,
3.	Gray, Hurst, Lewis and Meyer, "Analysis & Design of Analog ICs",4th Wiley, 2001

Detailed Syllabus
Lab-wise Breakup

Course Code	17M21EC113	**Semester ODD (specify Odd/Even)**	**Semester** 2nd **Session** 2018 -2019 **Month from** Jan to May
Course Name	Project Based Learning-I		
Credits	**2**	**Contact Hours**	**4**

Faculty (Names)	**Coordinator(s)**	Dr. Madhu Jain
	Teacher(s) (Alphabetically)	Dr. Garima Kapoor, Dr. Gaurav Verma, Mr. Mandeep Narula, Dr. Neetu Singh Ms. Ruby Beniwal, Ms. Smriti Bhatnagar

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO1	Demonstrate a depth of knowledge of Electronics and Microelectronics Engineering	Understanding (Level II)
CO2	Analyze various feasible methods of solving a problem to slot a suitable solution methodology	Analyzing (Level IV)
CO3	Demonstrate an ability to present and defend their research work to a panel of experts.	Evaluating (Level V)
CO4	Evaluate /Validate sound conclusions based on evidence and analysis	Create (Level VI)

Evaluation Criteria

(i)	Each fortnightly assessment (First assessment should be at the end of 3rd week from the beginning of the semester and thereafter fortnightly assessment. A total of six assessments giving a total percentage 6 x 8 = 48%)	-	48%
(ii)	Report at the end of the semester	-	10%
(iii)	Semester end presentation by the students	-	10%
(iv)	Viva-voce at the end of the semester	-	16%
(v)	Peer group evaluation (i.e. evaluation by the fellow students not belonging to the same batch)	-	8%
(vi)	Self assessment by the student concerned (can be moderated by the instructor by discussig with the student concerned)	-	8%

Detailed Syllabus
Lab-wise Breakup

Course Code	17M25EC112	Semester EVEN (specify Odd/Even)	Semester 2nd Session 2018 -2019 Month from jan to july 2019
Course Name	VLSI Design and Simulation Lab 2		
Credits	…	Contact Hours	…

Faculty (Names)	Coordinator(s)	Dr. Vikram Karwal
	Teacher(s) (Alphabetically)	Dr. Vikram Karwal

COURSE OUTCOMES		COGNITIVE LEVELS
CO1	At the end of the lab the student will understand the fault modeling in Digital Circuits (both combinational and sequential circuits)	Remember Level I
CO2	The student will be able to parse the given digital circuit using the standard design netlist ISCAS-85 for combinational circuits and ISCAC-89 for combinational circuits.	Understand Level II
CO3	The student will be able to implement the automatic test pattern generation algorithms and parse the netlist designed to compute the fault coverage.	Apply Level III
CO4	The student will be able to evaluate the given circuit for hard to oberserve and hard to control nets for the digital circuit under test.	Analyze Level IV
CO5	Student will be able to design partial scan and full scan design for testability techniques for sequential circuits.	Evaluate Level V
CO6	At the end of the lab the student will be able to design the layout in Mentor Graphics tool and simulate the behaviour	Create Level VI

Module No.	Title of the Module	List of Experiments	CO
1.	Exp.1	Getting familiarized with Synopsys Tools: Design Compiler, DFT Max, PrimeTime, TetraMax.	CO1
2.	Exp.2	Write netlist of a given combinational circuit using ISCAS-85 and induce the s-a fault to be parsed to ATPG algorithm to find fault coverage.	CO1
3.	Exp.3	Write netlist of a given sequential circuit using ISCAS-89 format and induce the s-a fault and find fault coverage using ATPG algorithms.	CO2
4.	Exp.4	To implement Roth's D-algorithm, Automatic test pattern generation algorithm in 'C/Python' programming language to generate test vectors for stuck-at faults in a given circuit (Input Netlist prepared in Exp.2 and find fault coverage).	CO3
5.	Exp.5	To implement Path Oriented Decision Making (PODEM) algorithm in 'C/Python' programming language and generate test vectors for stuck-at faults in a given circuit.(Use netlist prepared in exp. 2)	CO3
6.	Exp.6	Implement Sandia Controllability/Observability Analysis Program (SCOAP) and compute all controllability and oberservability measures for the netlist prepared in Exp. 3.	CO4
7.	Exp.7	Design for Testability (DFT), to implement partial scan design for the sequential circuit of Exp. 3 using primetime	CO5

8.	Exp.8	Design for Testability (DFT), to implement full scan design Design for Testability (DFT) for the sequential circuit designed in Exp 3 using primetime	CO5
9.	Exp.9	To design the layout of the Invertor using the Mentor Graphic tool.	CO6
10.	Exp.10	Study the DC and Transient Analysis of Inverter and Design rules for the invertor circuit designed in Exp. 9.	CO6

Evaluation Criteria

Components	Maximum Marks
Viva -120	
Viva -2 20	
D2D 60	
Total	100

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Bushnell Aggarwal, Springer
2.	Digital Systems Testing and Testable Design, Miron Abramovici, Melvin Breuer, Arthur Friedman
2.	Mentor Graphics, IC Station and Design Architect tutorial

Detailed Syllabus

Lecture-wise Breakup

Course Code	**19M13HS111**	Semester: **Even** (specify Odd/Even)	**Semester:** II **Session:** 2018 -2019 **Month from:** Jan-June
Course Name	**English For Research Paper Writing**		
Credits	2 (2-0-0)	**Contact Hours**	2
Faculty (Names)	**Coordinator(s)**	Dr Monali Bhattacharya	
	Teacher(s) (Alphabetically)	Dr Monali Bhattacharya	

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO1	To understand the aspects of grammar and language needed to write a paper.	Understand Level (C2)
CO2	To have improved Writing Skills with proper grammar usage	Apply level (C3)
CO3	To have knowledge of what to write in each section of a paper after careful analysis of Literature Review	Analyze Level (C4)
CO4	To be adept in skills needed to write a title, abstract and introduction, methods, discussion, results and conclusion	Evaluate Level (C5)
CO5	To be capable of drafting a refined research paper after editing and proofreading	Create Level (C6)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	Grammar & Usage	Structure of English Language Voice &Tense SVOCA Sense & Sense Relations in English Enhancing Vocabulary Connotation, Denotation & Collocation	6
2.	Elements of Paper Writing	Planning & Preparation Word Order Breaking Long Sentences Structuring Paragraphs Being Concise and Removing Redundancy	6
3.	Paraphrasing &	Highlighting Your Findings	4

	Writing	Paraphrasing and Plagiarism Sections of a Paper Abstracts; Introduction	
4.	Process of Writing	Review of Literature Methods Results Discussion Conclusion	4
5.	Key Skills Needed	Key skills needed when writing a Title Key skills needed when Writing an Abstract Key skills needed when writing an Introduction Key skills needed when writing a Review of the Literature Key skills needed when writing Methods & Results Key skills needed when writing Discussion & Conclusion	4
6.	Refining the Paper	Incorporating useful phrases Editing Proofreading References Annexures Ensuring good quality in submission	4
Total number of Lectures			**28**

Evaluation Criteria

Components	**Maximum Marks**
Mid Term Examination	30
End Semester Examination	40
TA	30 (Assignments)
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Goldbort R. 'Writing for Science', Yale University Press (available on Google Books), 2006
2.	Day R. 'How to Write and Publish a Scientific Paper', Cambridge University Press, 2006
3.	Adrian Wallwork. 'English for Writing Research Papers', Springer, New York, Dordrecht Heidelberg, London, 2011
4.	Yadugari M.A. ' Making Sense of English: A Textbook of Sounds, Words & Grammar' Viva Books Private Limited, New Delhi, 2013, Revised Edition
5.	Strauss, Jane. 'The Blue Book of Grammar and Punctuation, Josseybass, Wiley, San Francisco, 1999.