REGISTRATION FORM

Faculty Development Programme on

VLSI Chip Design Hands on using open source EDA

July 08, 2019 – July 12, 2019

1. Name:
2. Age & Date of Birth:
3. Designation:
4. Institution:
5. Address for Communication:

6. Contact Details

E-mail:

Phone No.: (with STD code)

Office:

Mobile:

7. EducationalQualification:
8. Subjects handled in last oneyear:

9. Professional Experience (in years)

Teaching:

Industry:

Signature of the Applicant

DECLARATION

The information provided by me is true to the best of my knowledge. I agree to abide by the rules and regulations governing the FDP. If selected, I shall attend the program for the entire duration.

Date:

Place:

Signature of the Applicant

SPONSORSHIP

Mr./ Ms./ Dr. …….

……

is an employee of our Institute / Organization and is hereby allowed to attend the FDP on **VLSI Chip Design Hands on using open source EDA** . He/She will be permitted to attend the program, if selected.

Date: Place:

Signature & Seal of the HOD/ Principal

***Soft copy of the registration form can be mailed to**

vijay.khare@jiit.ac.in

FDP through NKN Summer Course 2019

VLSI Chip Design Hands on using open source EDA

July 08, 2019 – July 12, 2019

Sponsored by

Ministry of Electronics and Information Technology (MeitY)

Organized by

Electronics and ICT Academy, National Institute of Technology, Patna

in association with

Jaypee Institute of Information Technology
(Deemed to be university under Section 3 of UGC Act 1956)

Department of ECE

A-10, Sector-62, Noida, U.P 201309, India

About Summer Courses:

Faculty Development Programmes in core areas of Electronics and Information & Communication Technology (ICT) streams have been planned by academies for delivery during Summers (i.e., May – July 2019). All these summer courses will be offered through National Knowledge Network (NKN) based Video Conferencing, with lectures delivered by invited experts from IITs, NITs, IIITs and other premier institutes/industries. In addition, local course coordinators at respective academies /identified remote centers will take care of sessions on design orientation/activity linked problems/ assignments/ case studies and quiz test(s). All seven EICT academies will host the participants simultaneously along with some selected remote centers all over our country, through NKN-VC infrastructure. Candidates could attend the training programme at Academy locations or at identified remote centers as per the convenience. For registration participants need to apply to one of the academies, however, they can attend the training programme at that academy or any remote centre attached to that respective academy, please refer to respective academy websites.

Target Beneficiaries:

Interested Faculty of engineering/technical institutions is eligible to attend these summer courses. Thirty (30) seats are available for each course to be offered at each academy/remote centre. Participants will be selected based on first-cum-first-serve basis by each academy. Selected participants will be communicated through e-mail / notified in E&ICT academy websites.

Registration Fees:

No Registration fee is charged for attending this programme planned at any designated academies/Remote centers. However, candidate should submit a DD of Rs.1000/- in favor of **"Director, NIT Patna; payable at Patna"** along with application form and the same will be handed over to the participant on the last day of the training. Certificate for participation as well as for satisfactory performance will be given to the participants subject to fulfillment of attending all sessions, submission of assignments and clearing the test(s).

How to apply:

Duly filled in form should reach the local coordinator along with DD in the address specified below. GoI norms will be followed for SC/ST participants. Softcopy of the registration form and DD can be mailed to vijay.khare@jiit.ac.in.

Course Duration:

The course is designed as 3 credit equivalent for 40 hours (Theory Lectures, Hands-on/Design orientation/Activity linked problems/Assignments Problem Solving/Case Studies sessions/Quiz Tests)

Key Topics:

- VLSI design, SOC Design
- Floorplanning & timing analysis
- Placement, Clock tree synthesis
- Global routing, Detailed routing
- Analog and Mixed Signal Circuits: Specifications, Design, Layout & GDS

Important dates:

Last date for application	: 05/07/2019
Intimation of Selection	: 06/07/2019

Accommodation & Travel:

Candidates have to arrange their own boarding and lodging. Only working lunch and snacks will be provided. No Travel Allowance will be paid to the participants.

Organizing Committee:

Dr. Gaurav Trivedi, IIT Guwahati
(Principal Coordinating Academy)
Dr. C. Periasamy, MNIT Jaipur
(Co-Principal Coordinating Academy)
Dr. Vijay Khare, JIIT, Noida
(Coordinator at remote centre)
Dr. Shamim Akhter, JIIT, Noida
(Lab faculty/Lab-In-charge)
Dr. Gaurav Verma, JIIT, Noida
NKN/VC faculty In-charge

Address for Communication:

Dr. Vijay Khare
Associate Professor, Department of ECE
Jaypee Institute of Information Technology
A-10, Sector-62, Noida, U.P 201309, India