विद्या तत्व ज्योतिसम:

Workshop

On

Low Voltage and Low Power VLSI Design

(August 22 – 23, 2014)

Organized by

Department of Electronics & Communication Engineering

Jaypee Institute of Information Technology, Noida
(Declared Deemed to be University under Section 3 of UGC Act 1956)

About the Institute

Jaypee Institute of Information Technology (JIIT), Noida was established in the year 2001 and has been declared as a "Deemed to be University" under Section 3 of UGC Act 1956. The institute was founded by revered Shri Jaiprakash Gaur ji and is run by Jaypee Sewa Sansthan with a vision to become a Centre of Excellence comparable to the best in the world for producing professionals with leadership quality in technology, innovation, entrepreneurship and management. The undergraduate programs of the university have been accredited by the National Board of Accreditation of AICTE. Well equipped modern laboratories and an intellectually stocked Learning Resource Centre with over 43750 books and 1.7 lacs e-Resources provide a pleasant and stimulating ambience. JIIT's state-of-the-art, environmentally conditioned campus comprises smart buildings with Wi-Fi connectivity covering the Academic Block, Business School cum Research Block, Faculty Residences, Student Hostels and Annapurna. For more information please visit: http://www.jiit.ac.in

About the Program

The workshop aims to deal with some of the very prominent design related issues in the field of low voltage and low power VLSI design. The challenges posed by aggressive voltage scaling will be discussed, and design guidelines to achieve robust operations will be taken up.

Low power has emerged as a major theme in the rapidly developing electronics industry. Power dissipation has become a critical design factor as it not only determines the thermal and electrical limits of designs; it also impacts the system cost, size and weight. Static power dissipation now constitutes a dominant component of the heat generated in VLSI chips. Sub-threshold conduction in the off-state of MOS switches, Gate Induced Drain Leakage, Gate-Tunneling and Junction Leakage contribute significantly to static power dissipation. Salient concepts related to above issues will be addressed in this workshop.

Design techniques that make possible the operation of analog circuits with ultra-low supply voltages, down to 0.5V will be demonstrated. The design of Operational Transconductance Amplifiers (OTAs) will be used as a vehicle to introduce these techniques. The OTAs include common-mode feedback and feed-forward circuits to allow maximum common-mode rejection. Automatic biasing strategies to maintain common-mode voltages and attain maximum signal-swing over process, voltage and temperature will also be discussed.

Speakers

- **Professor A.B. Bhattacharya** (Emeritus Prof., JIIT, Noida, Ex-Dean(IRD),and Head, CARE, IIT Delhi)
- **Professor G.S. Visweswaran** (Professor, Department of Electrical Engineering, IIT Delhi)
- **Dr. Kaushik Saha** (Director, Systems R&D, Samsung India)
- **Dr. Shouribrata Chatterjee** (Associate Prof., Department of Electrical Engineering, IIT Delhi)

Contents

- Issues & challenges in Low voltage & low Power VLSI Design
- Characteristics of scaled MOSFET with reference to down scaling of voltage and power.
- Sub-threshold and super threshold source/drain leakage current models for low-power scaled CMOS design
- Design of Operational Transconductance Amplifiers (OTAs)
- Sub 1- Volt Operational Amplifier Design
- Power Efficient Analog Circuit Design

Who Should Attend?

Active researchers, members of academia, scholars and professionals working in the VLSI domain.

Venue

Workshop will be held at: JIIT, Sector-128 campus, Jaypee Wish Town, Sector-128, NOIDA

Important Dates

Workshop Period: August 22-23, 2014
Last date of Registration: August 19, 2014.

Accommodation & Support

All the participants would be provided refreshments and lunch on each day of the workshop. Limited accommodation on twin sharing basis is available on a first come–first serve basis at a nominal rate of INR 200 per person per night.

Registration Details

A. Registration should be done online through the following link:
http://www.jiit.ac.in:8080/jiit/VLSIWorkshop/creditcard/RegisterationWorkshop2014.html

B. Registration Fee

- *Faculty Member:* INR 1500
- *Industry Professional:* INR 1500
- *Research Scholars/Students:* INR 500

C. Payment can be paid through any of the following modes:

1. Demand Draft (DD): DD in favor of "Jaypee Institute of Information Technology", payable at NOIDA should be sent to any of the resource persons mentioned in the next section.

2. Credit Card: To pay through Credit card, please visit the registration link given above.

Contact Persons

For any more information regarding the workshop, please contact:

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How To Reach JIIT, Sector-128 Campus, Noida

Metro: The station closest to the campus is Noida City Centre/Botanical garden. You can book reserved auto, available at metro station for JIIT, Sector-128, Noida.

Railway: Noida is well connected to the New Delhi Railway Station and the Old Delhi railway station by bus as well as by Metro. Autos can be hired just outside the railway stations.

Workshop Coordinators

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