Detailed Syllabus

Lecture-wise Breakup

Subject Code	16M3NEC361	**Semester: Even (specify Odd/Even)**	**Semester** II **Session** 2019- 20 **Month from** July 19 **to** Dec 19
Subject Name	Estimation over Distributed Networks		
Credits	3	**Contact Hours**	3

Faculty (Names)		**Coordinator(s)**	1. Vikram Karwal
		Teacher(s) (Alphabetically)	Vikram Karwal

S.No	Course Outcome	Cognitive levels/Blooms taxonomy
C121.1	To course aims to familiarize students with the importance of distributed adaptation, optimization and learning by multi-agent systems over distributed networks	Understanding Level (C2)
C121.2	The course aims to help student analyze efficient processing of Massive data using Distributed Networks.	Analyzing Level (C4)
C121.3	The course helps students understand, Importance and Need of distributed Networks.	Analyzing Level (C4)
C121.4	The course helps students to analyze local information available at individual nodes in a distributed manner.	Applying Level (C3)
C121.5	The students will be able to compute the computational complexity and compare various distributed algorithms.	Evaluating Level (C5)

Module No.	**Subtitle of the Module**	**Topics in the module**	**No. of Lectures for the module**
1.	Introduction and Background Material	Important matrix and Linear Algebra results, Convexity criterion, computation of complex Gradients and Hessian, Lipschitz conditions, regression, log-logistic cost function, mean-value theorems	6
2.	Single-Agent	Stochastic-gradient optimization,	6

	Adaptation and Learning	convergence and stability properties, constant and variable step size conditions, Mean-square error performance	
3.	Centralized Adaptation and Learning	Batch and centralized processing, convergence, stability and performance	5
4.	Multi-Agent Network Model	Importance of Distributed Networks vs. Centralized processing, distributed adaptation over networks, distributed learning over networks, optimization over distributed networks, importance of localized interactions among agents, their applications in social networks, biological networks.	9
5	Stability & Performance	Performance analysis of various estimation algorithms their convergence analysis, learning curves and their stability, robustness and resilience to failure, privacy and secrecy considerations among agents.	8
6.	Advanced Network Topologies	Benefits of co-operation, combination strategies, Role of Informed Agents, Adaptive Combination strategies, Asynchronous strategies, clustering	6
		Total number of Lectures	40

Evaluation Criteria	
Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25
Total	**100**

Recommended Reading material:	
1.	A. H. Sayed, *Adaptation, Learning, and Optimization over Networks,* NOW Publishers, 2014.
2.	S. Boyd, L. Vandenberghe, Convex Optimization, Cambridge University Press, 2004.
3.	T. Kailath, A. H. Sayed, B. Hassibi, Linear Estimation, Prentice Hall, 2000

Lecture-wise Breakup

Course Code	**18M11GE111**	**Semester** Odd	**Semester I** Month from	**Session** 2019 -2020 July to December
Course Name	Research Methodology & Intellectual Property Rights			
Credits	2	**Contact Hours**	2-0-0	
Faculty (Names)	**Coordinator(s)**	Prof. B. P. Chamola		
	Teacher(s) (Alphabetically)	Prof. B. P. Chamola		

COURSE OUTCOMES:		**COGNITIVE LEVELS**
After pursuing the above mentioned course, the students will be able to:		
C101.1	understand the basic concepts and types of research	Understanding Level (C2)
C101.2	define a research problem, its formulation, methodologies and analyze research related information	Analyzing Level (C4)
C101.3	follow research ethics, understand IPR, patents and their filing related to their innovative works.	Understanding Level (C2)
C101.4	understand and analyze the statistical data and apply the relevant test of hypothesis in their research problems	Analyzing Level (C4)

Module No.	Title of the Module	**Topics in the Module**	**No. of Lectures for the module**
1.	Research	What is research? Types of research. What is not research? How to read a Journal paper?	3
2.	Report writing	How to write report? Use of Mendeley in report writing. How to write a research paper? Problem identification and solving.	4
3.	Ethics, IPR and Research methodologies	Research ethics, patents, intellectual property rights, plagiarism regulation 2018. Steps in research process and common methodologies to attempt solution to research paper.	8
4.	Basics of statistics and probability distributions	Basic statistical concepts. Handling of raw data, Some common probability distributions.	7
5.	Test of hypothesis	Hypothesis testing. Parametric and non-	8

	and regression analysis	parametric data, Introduction to regression analysis.	
		Total number of Lectures (Course delivery method: open ended discussion, guided self-study, lectures)	**30**

Evaluation Criteria

Components	**Maximum Marks**
Mid Term Examination	30
End Semester Examination	40
Assignments	30 (Viva, Quiz, Assignments)
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	**Stuart Melville and Wayne Goddard**, Research Methodology: An Introduction for Science & Engineering Students, Kenwyn, South Africa : Juta& Co. Ltd., 1996.
2.	**Kothari, C.R.,** Research Methodology: Methods and Techniques, New Age International, New Delhi, 2009.
3.	**Kumar, Ranjit,** Research Methodology: A Step by Step Guide for Beginners, 2nd Edition, Sage Publications Ltd., 2005.
4.	**Ramappa, T.,** Intellectual Property Rights Under WTO, S. Chand, New Delhi, 2008.
5.	**Wayne Goddard and Stuart Melville,** Research Methodology: An Introduction, Kenwyn, South Africa : Juta& Co, 2001.

Detailed Syllabus

Lecture-wise Breakup

Course Code	**19M12EC112**	**Semester Odd semester (specify Odd/Even)**	**Semester Odd semester Session 2019-20** Month from July 2019 to Dec 2019.
Course Name	Dr.VijayKhare		
Credits	**3**	**Contact Hours**	**45**

Faculty (Names)	**Coordinator(s)**	Dr. Vijay Khare
	Teacher(s) (Alphabetically)	Dr. Vijay Khare

COURSE OUTCOMES		**COGNITIVE LEVELS**
CO120. 1	Explain soft computing techniques and their roles in building intelligent machines	Understanding(Level II)
CO120.2	Apply neural networks to pattern classification and regression problems	Applying (Level III)
CO120.3	Apply fuzzy logic and reasoning to handle uncertainty and solve engineering problems	Applying(Level III)
CO120.4	Apply genetic algorithms to combinatorial optimization problems	Applying (Level III)
CO120.5	Evaluate and compare solutions by various soft computing approaches for a real time problem use existing software tools.	Evaluating (Level V)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	Introduction	Introduction of soft computing .evolution of computing, hard computing and soft computing, soft computing methods.	2
2.	Fundamental of neural network	Introduction of neural network , Neuron models and n/w architecture Learning in Artificial Neural Networks; Supervised, Unsupervised and Competitive Learning paradigms, perceptron neural network: Adaline and Madaline	7
3.	Feed forward neural networkand applications	Multi layer Feed forward neural network, back propagation algorithms and radial basis neural network, Application of neural network	8
4.	Associated Memory	Auto associative memory, Hetro associated memory bidirectional associated memory	5
5.	Unsupervised learning	LVQ(Learning Vector Quantization) Self organization map, Adaptive resonance theory	6
6.	Fuzzy logic	Introduction, classical and Fuzzy sets &operations	9

		crisprelation and fuzzy relation Fuzzy rules based system, Fuzzy Controller Design	
7.	Genetic Algorithms	Introduction of Genetic Algorithms, Genetic Operators, Crossover and mutation properties, Genetic Algorithms in Problem Solving,	8
		Total number of Lectures	**45**

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1	Jacek M. Zurada, *Introduction to Artificial Neural Systems,Jaico Publishing House, 1994*
2	Martin T. Hagan, Howard B. Demuth, Mark Beale, *Neural Network Design-Martin Hagan,2014*
3	.SimonHykins, *Neural Networks-**A Comprehensive Foundation**Prentice Hall, 1999*
4	S. N. Sivanandam& S. N. Deepa, Principles of Soft Computing, Wiley - India, 2007
5	M. Mitchell, An Introduction to Genetic Algorithms, Prentice-Hall, 1998
6	Rajasekharan and Rai, *Neural Networks, Fuzzy logic, Genetic algorithms: synthesis and applications ,PHI-2003*

Detailed Syllabus
Lecture-wise Breakup

Subject Code	17M21EC111	**Semester**Odd	**Semester**I **Session**2019-20 **Month from** July**to** December
Subject Name	Microelectronic Devices Technology and Design Interface		
Credits	3	**Contact Hours**	3

Faculty (Names)	**Coordinator(s)**	Dr Saurabh Chaturvedi
	Teacher(s) (Alphabetically)	Dr Saurabh Chaturvedi

COURSE OUTCOMES - At the end of the course, students will be able to:		**COGNITIVE LEVELS**
C111.1	-Relate and recall the concepts of semiconductor physics, devices and technology	Remembering Level (C1)
C111.2	-Understand the MOS structure and explain the operation of MOS transistors	Understanding Level (C2)
C111.3	-Apply the knowledge of MOSFET scaling, short-geometry effects and fabrication techniques in advanced nanoscale devices and circuits	Applying Level (C3)
C111.4	-Analyze the device layout and characteristics -Analyze design flow and design interface	Analyzing Level (C4)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures**
1.	Semiconductor physics	Semiconductor materials, Energy bands, Intrinsic carrier concentration, Doping, Carrier drift and diffusion, Generation and recombination processes, Continuity equation, Thermionic emission process, p-n junction	11
2.	MOS capacitor	MOS structure, MOS system under external bias	7
3.	MOS transistor	Physical structure of MOS transistor, Types, Threshold voltage, MOSFET operation, Layout, MOSFET capacitances, SPICE models	11
4.	Scaling of MOS transistor	Types of scaling, Short-geometry effects, Introduction to SPICE model parameters	4
5.	Fabrication of MOS transistor	Basic steps, n-well CMOS process, Twin-tub technology	3

6.	Overview of CMOS/VLSI technology	CMOS technology, VLSI design methodologies, VLSI design flow, Design hierarchy, VLSI design styles	3
7.	Design interface	CMOS lambda-based design rules, Foundry interface	3
		Total number of lectures	42

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25
Total	**100**

Recommended Reading Material:

1. S. M. Sze, *Semiconductor devices: Physics and technology*, 2nd ed., John Wiley & Sons, 2009.
2. A. B. Bhattacharyya, *Compact MOSFET models for VLSI design*, 1st ed., Wiley-IEEE Press, 2009.
3. Y. Tsividis, *Operation and modeling of the MOS transistor*, 2nd ed., Oxford University Press, 2009.

Detailed Syllabus
Lecture-wise Breakup

Course Code	13M1NEC338	**Semester Odd (specify Odd/Even)**	**Semester** Ist **Session** 2019-20 **Month from** July **to** December
Course Name	VLSI Physical Design		
Credits	3	**Contact Hours**	3-0-0

Faculty (Names)	**Coordinator(s)**	Dr. Shruti Kalra
	Teacher(s) (Alphabetically)	

COURSE OUTCOMES		**COGNITIVE LEVELS**
C141.1	Recall the basics of IC design	Remembering Level (C1)
C141.2	Understand the process of VLSI layout design	Understanding Level (C2)
C141.3	Applying the basic physical design algorithms for VLSI circuits.	Applying Level (C3)
C141.4	Analyze the physical design automation techniques used in the best-known academic and commercial layout systems.	Analyzing Level (C4)

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	Introduction	VLSI Design Flow, Understanding VLSI design problem, Different Design Domains, Design Actions, Design Methods, Technology used, Full custom, Semi Custom, Introduction to FPGA, ASIC, IP Cores, Importance of CAD in VLSI with respect to each design stage.	3
2.	Physical Design process	Physical Design cycle, Physical Design cycle for ASICs and FPGA, Concept of translation of circuits into geometry, Types of algorithms used to achieve physical design stages, Problems associated with physical design process (parasitic delay, interconnect delay, noise/cross talk, process shifting etc), Understanding timing issues in digital circuits and systems (set up time, hold time, clock skew, jitter, slack)	8
3.	Algorithms and Data Structures	Algorithm Analysis – Complexity of algorithms, Asymptotic notation (big O), Basic Algorithms - sorting	8

		algorithms, Binary search algorithms,Graph Algorithms- shortest path algorithms, Steiner Tree Algorithm,Computational Geometry Algorithms -plane sweep technique ,Data Structures- Binary Search trees, AVL trees, Range trees, Graphs, stacks and queues	
4.	Design Rule Checking	Size rule, separation rule, overlapping rule, use of plane sweep technique to perform design rule checking	3
5.	Partitioning Algorithms	Problem formulation, K-L algorithm, F-M algorithm, Simulated Annealing	5
6.	Floor Planning and Placement Algorithms	Problem formulation, simulation based algorithms	4
7.	Routing Algorithms	Problem Formulation, global routing algorithms and detailed routing algorithms	7
8.	Compaction Algorithms	Problem Formulation, classification of compaction analysis, one and two dimensional compaction algorithms.	4
		Total number of Lectures	41

Evaluation Criteria

Components	**Maximum Marks**
T1	20
T2	20
End Semester Examination	35
TA	25
Total	**100**

Recommended Reading material: (Books/Journals/Reports/Websites etc.: Author(s), Title, Edition, Publisher, Year of Publication etc. in IEEE format)

1.	Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic, 1998.
2.	Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Mc-Graw Hill, 1994.
3.	"The Best of ICCAD: 20 Years of Excellence in Computer-Aided Design", Andreas Kuehlmann editor, Kluwer Academic Publishers, 2002.
4.	Michael T. Goodrich and Roberto Tamassia, "Algorithm Design" Wiley
5.	Sabih H. Gerez, "Algorithms for VLSI Design Automation" Wiley

Detailed Syllabus
Lecture-wise Breakup

Course Code	**17M21EC112**	**Semester ODD (specify Odd/Even)**	**Semester ODD Session 2019 - 2020 Month from July - December**
Course Name	**Digital Integrated Circuit Design**		
Credits	**3**	**Contact Hours**	**3**

Faculty (Names)	**Coordinator(s)**	**Dr Amit Kumar Goyal**
	Teacher(s) (Alphabetically)	**Dr Amit Kumar Goyal**

COURSE OUTCOMES		**COGNITIVE LEVELS**
C112.1	**Develop an understanding of exiting challenges in digital IC design, and analysis of CMOS inverter performance.**	**Understanding (Level II)**
C112.2	**Identify and estimate the delay and power consumption in CMOS based gates and choosing best design configuration via logical effort.**	**Analyzing (Level IV)**
C112.3	**Design and analyze combinational and sequential logic circuits effectively.**	**Applying (Level III)**
C112.4	**Design different types of semiconductor memories and test integrated circuits for fault tolerance.**	**Evaluating (Level V)**

Module No.	**Title of the Module**	**Topics in the Module**	**No. of Lectures for the module**
1.	**Introduction to CMOS digital integrated circuits**	**Digital integrated circuit basic: cost, reliability, yield and performance, Challenges in DIC design, CMOS devices and manufacturing technology and design rules, CMOS inverters and gates, Propagation delay calculation of CMOS inverter, noise margins, power dissipation, and regenerative logic circuits**	**10**
2.	**Delay Estimation and Power consumption in CMOS gates**	**Delay Definitions, Switch-level RC Delay Models, Effective Resistance and Capacitance calculations, Elmore Delay Model, Linear Delay Model, Switching Activity of logic gates**	**7**
3.	**Logical Effort**	**Delay in a Logic gate, Multistage Logic Networks, Gate sizing, Choosing the best No. of stages, Limitation of logical effort**	**6**
4.	**Designing Arithmetic Building Blocks**	**Complex CMOS circuit design, Static and dynamic logic, Adders, Multipliers and Shifters**	**8**
5.	**Sequential Circuit Analysis**	**Timing Metrics for Sequential Circuits, Bi-stability principle, Static latches and Registers, Flip flops,**	**7**

		Dynamic Sequential Circuit, Schmitt Trigger	
6.	Designing Memory and Array Architecture	Semiconductor Memories, Memory peripheral Circuitry	4
7.	Testing	Introduction to testing and various concepts	4
		Total number of Lectures	46

Evaluation Criteria

Components	Maximum Marks
T1	20
T2	20
End Semester Examination	35
TA	25 (Two Assignment and One Quiz)
Total	100

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	J. M. Rabaey, A. Chandrakasan, B. Nikolic: Digital Integrated Circuit: A design perspective, 2nd Edition Pearson Education, Delhi-2005
2.	Weste, Neil HE, and David Money Harris. CMOS VLSI Design. Pearson/Addison Wesley, 2005. Geiger,
3.	Randall L., Phillip E. Allen, and Noel R. Strader. VLSI design techniques for analog and digital circuits. Vol. 90. New York: McGraw-Hill, 1990.
4.	www.ieeexplore.ieee.org

Detailed Syllabus
Lab-wise Breakup

Course Code	**17M25EC111**	**Semester** Odd **(specify Odd/Even)**	**Semester** Ist **Session** 2019 -2020 Monthfrom July 2019 to Dec 2019
Course Name	VLSI Design and Simulation Lab-I		
Credits	3	**Contact Hours**	6

Faculty (Names)	**Coordinator(s)**	Rachna Singh
	Teacher(s) (Alphabetically)	Gaurav Verma, Rachna Singh, Saurabh Chaturvedi, Shamim Akhter

COURSE OUTCOMES: At the end student will be able to		**COGNITIVE LEVELS**
C170.1	Understanding the fundamental concepts of C programming, architecture and interfacing of on chip and external peripherals with AT89C51 micro controller	Understanding (Level II)
C170.2	Apply the concept of embedded 'C' programming & interfacing in designing embedded application around various sensors and Actuotors.	Applying (Level III)
C170.3	Experiment the embedded system designs on simulator & development board.	Analyzing (Level IV)
C170.4	UseEDA tool for VLSI circuit design	Understanding (Level II)
C170.5	Apply the MOS device theory to obtain the MOS I-V characteristics and perform parameter extraction	Applying (Level III
C170.6	Analyze the static and switching characteristics of MOS-based circuits	Analyzing (Level IV)

Module No.	**Title of the Module**	**List of Experiments**	**CO**
1.	Familiarization with 8051 Kit and related software like Keil &ProgISP	To get acquainted with the board, peripherals and subsequently write the programs like i) Blinking of LED ii) Control of LED using tactile/momentary switch.	CO1
2.	Concept of PWM	Generate a Square wave of 50% duty cycle and test on scope.	CO1
3.	Token Display system	Design a Token display system that has seven segment display and switches. Whenever any switch is pressed corresponding number is displayed on the segment.	CO2
4.	Traffic Light Controller	Design a traffic light controller system that has four LEDs- RED, YELLOW. GREEN and ADVANE	CO2

		GREEN. The sequence in which the LEDs are turned on is as follows: RED for 1 min, YELLOW for 15 sec, GREEN for 1 min, ADVANE GREEN for the last 10 sec of GREEN. Interface a light dependent resistor(LDR) to select manual and automatic mode.	
5.	Real Time Clock/Date Display	Design a digital clock display using LCD and a mode switch. The clock, normally displays the time in hr-min-sec format. It updates the time automatically using the timer interrupt of the microcontroller. On pressing the mode switch, the display changes to date in dd-mm-yy format. . On pressing the button, the display returns to show time.	CO2
6.	DC motor interfacing using relay with IR sensor interface	Interface a DC motor with the microcontroller. The system will have two IR sensors. Initially, the motor is at zero speed. With every flash of the IR, the speed will increase by a fixed amount. After eight such flashes, it returns to zero speed. The other IR sensor is used to toggle the direction of rotation of the motor.	CO2
7.	Wave form Generation using DAC	Interface a DAC0808 chip with microcontroller and generate different waveforms, such as i) sinusoidal ii) triangular iii) saw-tooth.	CO3
8.	ADC Interfacing	Design a temperature monitoring and control system consist of a temperature sensor, dc fan, relay and a heating coil. If temp>higher cutoff, coil should be turned off & fan should be on. If temp<Lower cutoff, coil should be turned on & fan should be off.	CO3
9.	Interfacing of DTMF Module	Do the following task using your mobile phone wired/wireless. i) Display " JIIT NOIDA" on LCD on pressing 1 ii) Rotate stepper motor clockwise on pressing 2 iii) Rotate stepper motor anticlockwise on pressing 3.	CO3
10.	Serial/Wireless communication between kits two kits	Interface two 8051 kits using UART/Zigbee for data transfer.	CO3
11.	Introduction to CAD/EDA tool	Introduction to Tanner tools: T-Spice, S-Edit and L-Edit.	CO4
12.	Analysis of MOS transistors	To study the I-V characteristics of MOS transistors and perform parameter extractions.	CO5
13.	DC analysis of MOS inverters	To analyze the voltage transfer characteristics (VTC) of MOS based inverters and then calculate critical points	CO6
14.	Transient analysis of MOS-based	To analyze and calculate the propagation delay, rise time and fall time of a CMOS inverter.	CO6

	combinational circuits	Simulate the logic gates and verify the truth tables:Two-input NAND, two-input NOR. Simulation of a logic circuit with the given Boolean expression. Implementation of a two-input XOR gate and 2X1 multiplexers using CMOS transmission gates. Implementation of a two-input multiplexer using sub-circuit technique.	

Evaluation Criteria

Components	**Maximum Marks**
Viva1	20
Viva2	20
Day to Day	60
Total	**100**

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	S.-M. Kang and Y. Leblebici, "CMOS digital integrated circuits: Analysis and design," 3rd edition, Tata McGraw-Hill, 2003.
2.	N. H. E. Weste and D. M. Harris, "CMOS VLSI design: A circuits and systems perspective," 3rd edition, Addison-Wesley, 2005.
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