NXP CAMPUS CONNECT

SESSION IS HOSTED BY
JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY

Physical Design and STA

LIVE SESSION

This session will cover overall Physical design and static timing analysis flow in SoC backend design including overview of Synthesis, APR and STA functions. Purpose and goal of various implementation stages i.e., Floorplan, Placement, CTS and Routing, STA will be discussed in the session. This topic gives the audience introduction to backend design fundamentals, associated challenges and also talks about good implementation techniques.

SPEAKERS

PUNEET SHAH
Senior Principal Manager
NXP Semiconductors

RUPESH BAMANE
Director Engineering
NXP Semiconductors

Attend the session in-person

Or Join Virtually

Tuesday	June 06
5:00 – 6:30 pm IST	LT4 Hall

Write to us at: nxpcampus.connect@nxp.com

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RUPESH BAMANE
Director Engineering

PUNEET SHAH
Senior Principal Manager

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Speaker Announcement

RUPESH BAMANE

Rupesh manages the MMEDE STA signoff team in NXP, Bangalore and has been in the industry for 17+ years. His role includes engaging with Technology and Design Enablement teams, aligning on timing signoff criteria, work with Physical implementation teams for timing closure and signoff. Beyond work, Rupesh likes to spend time in Algo Trading as a hobby and spend time with family and friends.

PUNEET SHAH

Puneet works as Senior Principal Manager in MMEDE R&D Organization at NXP, Bangalore. He handles SoC implementation and hard macro teams that work on MPU design. He has 14+ years of experience in various leadership and physical design lead roles in SoC implementation.

Join us for the webinar on

Physical Design and STA
06th June 2023 at 5.00 – 6.30 PM

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